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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,746	07/10/2001	Yoshinori Takahashi	36856.526	8463

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/901,746	TAKAHASHI, YOSHINORI	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8,10-15 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,10-15 and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *18032004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is responsive to the amendment filed on 01-21-04. Applicant's arguments with respect to references of Mandai et al. (US Pat.5, 227,739) have been carefully considered but they are not deemed to be persuasive to overcome the references. Thus the claims remained rejected under Mandai.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3-7, 8, 10-13, 14, 15 and 17-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claims 1, 8 and 14, the recitation: "**one** of the omitted portions is aligned with the through hole and **another** of the omitted portions is aligned with the micro-strip line" is indefinite because it is misdescritive. Figure 2 of the present application shows that there is **only one** omitted portion (32) and **two** through holes (30, 30). The omitted portion (32) is aligned with the microstrip (28) and two through holes (30), (30) are aligned with each other. There **is no** "another of the omitted portion" that is aligned with the through hole (30). Therefore, the recited connection of **two** omitted portions is misdescriptive.

Claims 3-7, 10-13, 15 and 17-21 are misdescriptive because of the technical deficiencies of claims 1, 8 and 14.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-8, 10-15 and 17-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Mandai et al. (US Pat. 5,227,739).

Regarding claim 1, figure 4 of Mandai shows a resonator comprising: a multi-layer substrate having an upper and lower surface, and including at least two grounding conductor

layers (3, 5, 7) and a plurality of dielectric layers (2a-2g), one of the at least two grounding conductor layers (3) being disposed on the lower surface of the multi-layer substrate; a strip line (4) disposed between the at least two grounding conductor layers (3,5); a microstrip line (9) disposed on the upper surface of said multi-layer substrate; and a through hole (V1) formed in said dielectric layers (2f) to connect said strip line (4) to said microstrip line (9); wherein the rectanglular portions of the one (7) of the at least two grounding conductor layers (5, 7) that is closest to said microstrip line (9) are omitted. The omitted portions are aligned with the through hole (V1, inside the rectanglular omitted portion) and the microstrip (9). Note that there is a plurality of omitted portions and through holes (V1). The through hole is inside omitted portion and sharing the same vertical axis thus; the through hole (V1) is aligned with the omitted portion (rectanglular opening).

Regarding claims 3 and 4, figure 4 of Mandai shows that the rectangular omitted portions are defined in the grounding conductor layer (5 or 7).

Regarding claim 5, the strip line (4) has an U-shaped configuration.

Regarding claims 6 and 7, the resonator comprises only one strip line (4) and one micro-strip line (9).

Regarding claim 8, 10, 11, 12 and 13, figure 4 of Mandai shows a resonator comprising:

a multi-layer substrate having an upper and lower surface, and including at least two grounding conductor layers (3, 5, 7) and a plurality of dielectric layers (2a-2g), one of the at least two grounding conductor layers (3, 5) being disposed on the lower surface of the multi-layer substrate, and one of the at least two grounding conductor layers (5, 7) that is closest to said micro-strip line has rectangular openings formed therein;

a strip line (4) disposed between the at least two grounding conductor layers (3, 5);

a microstrip line (9) disposed on the upper surface of said multi-layer substrate; and

a through hole (V1) formed in said dielectric layers to connect said strip line to said microstrip line ; wherein the rectangular openings are "aligned" with the through hole (V1) and the microstrip (9). Note that there is a plurality of rectangular omitted portions (openings) and through holes (V1). The through hole is inside omitted portion, thus the through hole is aligned with the omitted portion (opening). The grounding conductor layer (3) faces the strip line (4).

The opening has a rectangular shape and the strip line (4) has an U- shaped configuration. The resonator comprises only one strip line and a microstrip line (9).

Regarding claims 14 and 15, figure 4 of Mandai shows a voltage controlled oscillator comprising: a resonator including:

a multi-layer substrate having an upper and lower surface, and including at least two grounding conductor layers (3, 5, 7) and a plurality of dielectric layers (2a-2g), one of the at least two grounding conductor layers being disposed on the lower surface of the multi-layer substrate;

a strip line (4) disposed between the at least two grounding conductor layers;

a microstrip line (9) disposed on the upper surface of said multi-layer substrate; and

a through hole (V1) formed in said dielectric layers to connect said strip line to said microstrip line;

wherein portions rectangular portion of the one of the at least two grounding conductor layers (5, 7) that is closest to said microstrip line (9) are omitted. The omitted rectangular portions are aligned with the through hole and the microstrip (9). Note that there is a plurality of omitted portions and through holes (V1). The through hole is inside the rectangular omitted portion, thus the through hole is aligned with the rectangular omitted portion (opening).

a plurality of electronic component elements disposed on the upper surface (2g) of the multi-layer substrate and arranged to define a circuit and inherently the plurality of the electronic component elements and the resonator are electrically connected to each other.

Regarding claims 17, the rectangular omitted portions define openings in said one of the at least two grounding conductor layers (3, 5, 7).

Regarding claims 18 and 19, the strip line (4) has a U shape and the openings have a substantially rectangular shape or square shape.

Regarding claims 20 and 21, the voltage-controlled oscillator comprises only one micro-strip line (9) or only one strip line (4).

Response to Arguments

Regarding the 112, 2nd paragraph issue, in the Remarks, page 9, first paragraph, the Applicant argues that in figure 2 of the present application, the two omitted **portions** are the

removed portion 32 and the **through hole** 30 and "one of the **omitted portions** is aligned with the **through hole** and another of the omitted portions is aligned with the microstrip line". This is not seen in the preferred embodiment since "element" (30) cannot be both a through hole and an omitted portion. According to figure 2, the omitted portion (32) is aligned with the microstrip line (28) and the **two through holes** (30, 30) are aligned with each other. Therefore, claims 1, 8 and 14 are remain misdescriptive because figure 2 shows that there are only **one** omitted portion (32) and two through holes (30, 30).

In page 11, first paragraph, the Applicant argues that element (9) is not a microstrip line. By definition, a microstrip line or a stripline is a planar structure consisting of the dielectric substrate, **a conductor strip** for the conductor pattern on one side of the substrate..." (see attached documents). Element (9) in figure 4 of Mandai is a conductor strip that meets all the definitions of a micro-strip thus, element (9) is a micro-strip. The microstrip is also called a stripline.

In page 11 of the Remark, 2nd paragraph, the Applicant also argues that " the **omitted portions** of Mandai et al. **are not through holes**". Figure 4 of Mandai shows that the through holes (V1) on layer (7) is not the omitted portion that is a rectangular cut out on the grounding conductor. This omitted portion is aligned with the through hole (V1). Moreover, figure 2 of the present application shows that the omitted portion (32) is **not** the through hole (30) and the claims do not recite that the omitted portions **are** through holes. In fact the claims recite that "one of the omitted portions **is aligned** with the through hole".

Conclusion

THIS ACTION IS MADE FINAL See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
03-18-04

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